Abstract of the Disclosure

A memory array with memory cells arranged in rows and columns with each cell having twin EEPROMs featuring subsurface stepped floating gates for electric field concentration. The twin EEPROMs employ only a single layer of poly, one portion being a floating gate of each EEPROM and another portion being word lines. The twin EEPROMs share a common subsurface electrode by having diffused control lines and a diffused bit line. The two EEPROMs are symmetric across the common electrode.